PTB48600 —48-V Input

85 W Dual Complementary-Output DC/DC Converter for DSL

SLTS239 JANUARY 2005

Features

- Dual Complementary Outputs (±5 V)
- Input Voltage Range: 36 V to 75 V
- On/Off Enable for Sequencing
- 1500 VDC Isolation
- Over-Current Protection
- Over-Temperature Shutdown
- Under-Voltage Lockout
- Temp Range: –40 to +85°C
- Fixed Frequency Operation
- Synchronizes with PTB4850x
- Powers line driver ICs for AC-7 and other xDSL chipsets
- Safety Approvals: (Pending)
  EN60950
  UL/cUL60950

Description

The PTB48600A is one of a series of isolated DC/DC converter modules that provide a pair of complementary supply voltages for powering line-driver ICs in xDSL telecom applications. These modules operate from a standard telecom (-48 V) central office supply and can provide up to a 85 W of power in a balanced load configuration.

The A-suffix module (±5 V) is designed to power the line driver ICs for the AC-7 ADSL chipset. It will also power any other applications that require a complementary supply with relatively balanced loads. The two compliementary outputs can also be configured as a single output of twice the voltage magnitude. As an example, the outputs of a PTB48600A can be adjusted up to ±6 V, and configured as a single 12-V output.

The PTB48600 includes an output "on/off" enable control, output current limit, over-temperature protection, and input under-voltage lockout (UVLO).

The control inputs, "Enable" and "Sync In," are compatible with the "EN Out" and "Sync Out" signals of the PTB4850x DC/DC converter. This allows the power-up and switching frequency of a PTB48600 module to be directly controlled from a PTB48500. Together the PTB48500 and PTB48600 converters meet all the system power and sequencing requirements of the AC-7 ADSL chipset.

The PTB48600 employs double-sided surface mount construction. The package options include both through-hole and surface mount pin configurations.

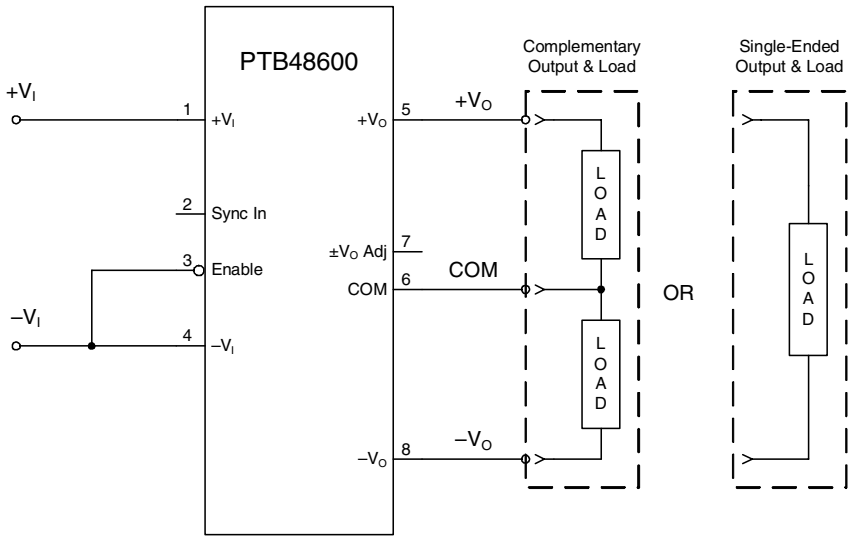
Pin Configuration

Pin	Function
1	$+V_I$
2	Sync In
3	Enable *
4	$-V_I$
5	$+V_O$
6	COM
7	V_O Adjust
8	$-V_O$

Shaded functions indicate signals that are referenced to –Vin.

* *Denotes negative logic:*
Open = Outputs Off
–Vin = Normal operation

Stand-Alone Application



Ordering Information

Base Pt. No. (PTB4860❒xxx)

Order Prefix	Description
PTB48600xxx	Basic Model

Output Voltage (PTB48600❒xx)

Code	Voltage
A	±5 V

Package Options (PT48600A❒❒)

Code	Description	Pkg Ref. (1)
AH	Horiz. T/H	(ERT)
AS	SMD, Standard (2)	(ERU)

Notes: *(1) Reference the applicable package reference drawing for the dimensions and PC board layout*
(2) "Standard" option specifies 63/37, Sn/Pb pin solder material.

Pin Descriptions

+V_I: The positive input supply for the module with respect to –V_I. When powering the module from a –48 V telecom central office supply, this input is connected to the primary system ground.

–V_I: The negative input supply for the module, and the 0 VDC reference for the '*Enable**', and '*Sync In*' signals. When the module is powered from a +48-V supply, this input is connected to the 48-V Return.

+V_O: The positive output supply voltage, which is referenced to the '*COM*' node. The voltage at '+V_O' has the same magnitude, but is the complement to that at '-V_O'.

–V_O: The negative output supply voltage, which is referenced to the '*COM*' node. The voltage at '-V_O' has the same magnitude, but is the complement to that at '+V_O'.

COM: The secondary return reference for the module's regulated output voltages. This node is dc isolated from the input supply pins.

±V_O Adjust: Using a single resistor, this pin allows the magnitude of both '+V_O' and '–V_O' to be adjusted together, either higher or lower than their preset value. If not used, this pin should be left open circuit.

Enable*: This is an open-collector (open-drain) negative logic input that enables the module output. This pin is referenced to -V_I. A logic '0' at this pin enables the module's outputs, and a high impedance disables the outputs. If this feature is not used the pin should be connected to –V_I. *Note: Connecting this input directly to the "EN Out" pin of the PTB4850x enables the output voltages from both converters (PTB4850x and PTB48600) to power up in sequence.*

Sync In: This pin is used when the PTB48600 and PTB4850x DC/DC converter modules are used together. Connecting this pin to the '*Sync Out*' of the PTB4850x module allows the PTB48600 to be synchronized to the same switch conversion frequency as the PTB4850x.

Environmental and General Specifications (Unless otherwise stated, all voltages are with respect to –V_I)

Characteristics	Symbols	Conditions		Min	Typ	Max	Units
Input Voltage Range	V_I	Over output load range		36	48	75	VDC
Isolation Voltage Capacitance Resistance		Input–output/input–case Input to output Input to output		1500 — 10	— 1500 —	— — —	V pF MΩ
Operating Temperature Range	T_A	Over V_{in} Range		–40	—	+85	°C
Over-Temperature Protection	OTP	Shutdown threshold Hysterisis		— —	115 (i) 10	— —	°C
Solder Reflow Temperature	T_{REFLOW}	Surface temperature of module body or pins				235 (ii)	°C
Storage Temperature	T_S	—		–40	—	125	°C
Mechanical Vibration		Mil-STD-883D, Method 2007.2 20-2000 Hz	T/H SMD	— —	20 2.5	— —	G's
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted	T/H SMD	— —	500 250	— —	G's
Weight	—			—	35	—	grams
Flammability	—	Meets UL 94V-O					

Notes: *(i) This parameter is defined by design*
(ii) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

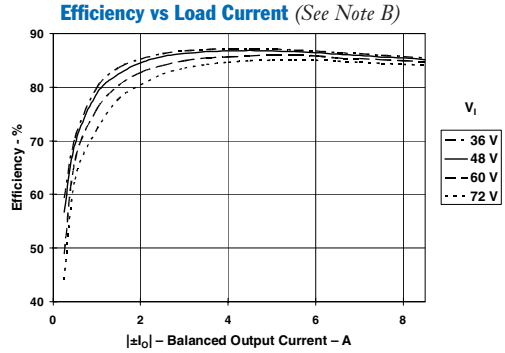
Specifications (Unless otherwise stated, T_A =25°C, V_I =48 V, C_I =0 µF, ±C_O =0 µF, $|+I_O|$ = $|-I_O|$, and $|\pm I_O|$ =0.5 $|\pm I_O|_{max}$)

Characteristic	Symbol	Conditions	PTB48600A Min	Typ	Max	Units
Output Power	P_O	Total output power from $\pm V_O$	0	—	85 (1)	W
Output Current	$\|\pm I_O\|$	Over V_I range, $\|+I_O\| - \|-I_O\| \le 0.1$ A	0	—	8.5 (2)	A
Output Load Imbalance	$\|+I_O\| - \|-I_O\|$	$\|+I_O\| \ge 0.1$ A, $\|-I_O\| \ge 0.1$ A	0	—	1 (3)	A
Output Voltage	$\|\pm V_O\|$	Inlcudes set-point, line, $\|+I_O\| - \|-I_O\| \le 0.1$ A $-40 \le T_A \le +85$°C	4.75 (2)	5	5.25 (2)	V
Temperature Variation	ΔReg_{TEMP}	$-40 \le T_A \le +85$°C, $\|\pm I_O\|$ =0.1 A $+V_O$ $-V_O$	— —	±1 ±1	— —	$\%V_o$
Line Regulation	ΔReg_{LINE}	Over V_I range, balanced load $\pm V_O$	—	±0.1	±0.4	$\%V_o$
Load Regulation	ΔReg_{LOAD}	Over $\pm I_O$ range, balanced load $\pm V_O$	—	±0.2	±0.4	$\%V_o$
Efficiency	η		—	85	—	%
V_o Ripple (pk-pk)	$\pm V_R$	20 MHz bandwidth, C_O =10 µF tantalum capacitor	—	20	30 (4)	mV_{pp}
Transient Response	t_{TR}	0.1 A/µs load step, 50% to 75% $\pm I_O$max	—	30	—	µs
	ΔV_{TR}	$\|\pm V_O\|$ over/undershoot	—	±1	—	$\%V_o$
Over Current Threshold	$\|\pm I_O\|$ trip	V_I =36 V, $\|+I_O\| = \|-I_O\|$, reset followed by auto-recovery	9	10	12	A
Short Circuit Current		Continuous over-current trip, $\|\pm I_O\|_{PK}$	—	16	—	A
		$\|+I_O\| = \|-I_O\|$ Duty	—	10	—	%
Output Voltage Adjust Range	$\|\pm V_O\|$ adj	$\|+V_O\|$ and $\|-V_O\|$ adjust simulataneously	3.31	—	6	V
Switching Frequency	f_S	Over V_I and I_O ranges	440	470 (5)	500	kHz
Under-Voltage Lockout	V_I on V_I off	V_I increasing V_I decreasing	— —	33 32	— —	V
On/Off Enable (pin 3) Input High Voltage Input Low Voltage	 V_{IH} V_{IL}	Referenced to $-V_I$ (pin 4)	 +3.6 –0.2	 — —	 +75 (6) +0.8	V
Input Low Current	I_{IL}		—	—	–1	mA
Standby Input Current	I_I standby	pin 3 open circuit	—	2	—	mA
Start-up Time	t_{ON}	$\|\pm I_O\|$ =1 A, $\|\pm V_O\|$ rising 0 to 0.95 $\|\pm V_O\|$ typ	6	10	22	ms
Internal Input Capacitance	C_I		—	3	—	µF
External Output Capacitance	±C_O	Capacitance from either output to COM	0	—	5,000 (7)	µF
Reliability	MTBF	Per Telcordia SR-332 50% stress, T_A =40°C, gnd benign	2.8	—	—	10^6 Hrs

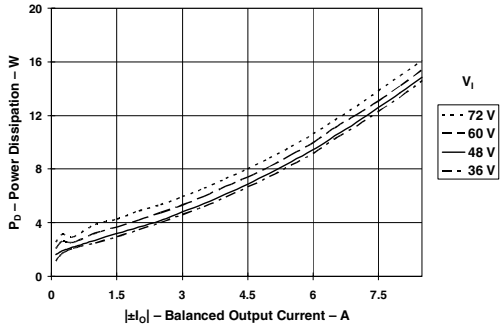
Notes: *(1) See Safe Operating Area curves or contact the factory for the appropriate derating.*
(2) Under balanced load conditions, load current flowing out of $+V_O$ is balanced to within ±0.1 A of that flowing into $-V_O$.
(3) A load imbalance is the difference in current flowing from $+V_O$ to $-V_O$. The module can operate with a higher imbalance but with reduced specifications.
(4) Output voltage ripple is measured with a 10 µF tantalum capacitor connected from $+V_O$ (pin 5) or $-V_O$ (pin 8), to COM (pin 6).
(5) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
(6) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to $+V_I$. The open-circuit voltage is 5 V max. If it is left open circuit the converter will operate when input power is applied.
(7) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

PTB48600A Characteristic Data @V_{IN} =48 V *(See Notes A)*

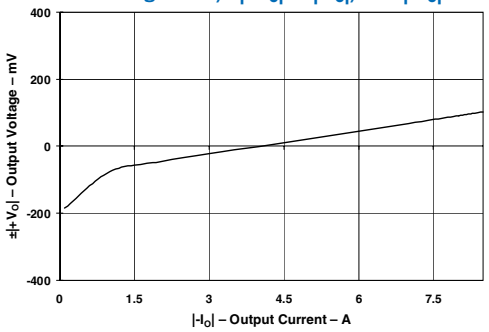
Efficiency vs Load Current *(See Note B)*



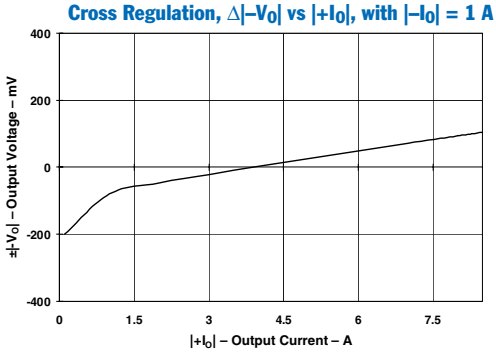
Power Dissipation vs Load Current *(See Note B)*



Cross Regulation, Δ|+V_O| vs |–I_O|, with |+I_O| = 1 A

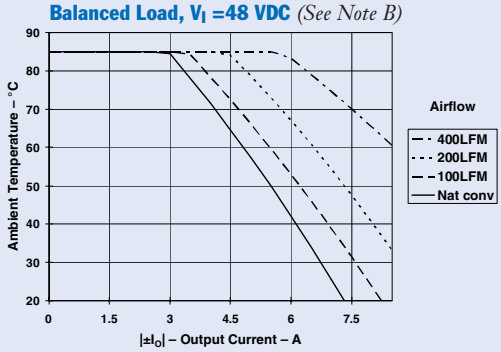


Cross Regulation, Δ|–V_O| vs |+I_O|, with |–I_O| = 1 A



Safe Operating Area PTB48600A *(See Note C)*

Balanced Load, V_I =48 VDC *(See Note B)*



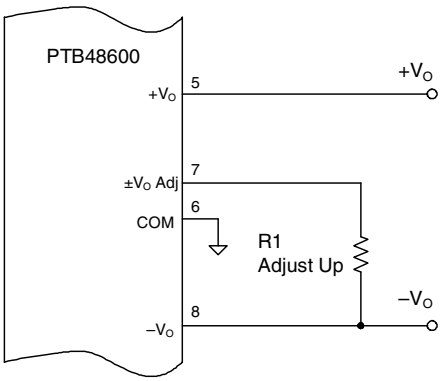
Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.*
Note B: *Under a balanced load, current flowing out of $+V_o$ is equal to that flowing into $–V_o$.*
Note C: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.*

Adjusting the Output Voltages of the PTB48600 Series of DC/DC Converters

The PTB48600 DC/DC converter produces a balanced pair of complementary output voltages. They are identified $+V_O$ and $-V_O$, respectively. The magnitude of both output voltages can be adjusted together as a pair, higher or lower. The adjustment method uses a single external resistor. [1] The value of the resistor determines the adjustment magnitude, and its placement determines whether the magnitude is increased or decreased. The resistor values can be calculated using the appropriate formula (see below). The formula constants are given in Table 1-1. The placement of each resistor is as follows.

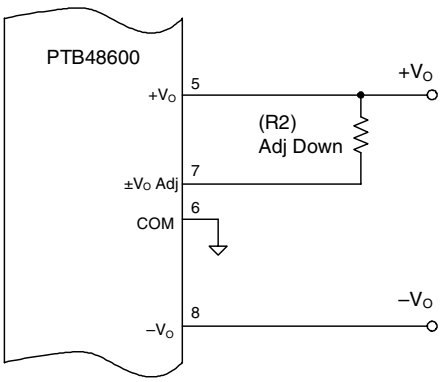
Adjust Up: To increase the magnitude of both output voltages, place a resistor R_1 between $\pm V_O$ *Adj* (pin 7) and the $-V_O$ (pin 8) voltage rail; see Figure 1-1(a).

Figure 1-1a



Adjust Down: To decrease the magnitude of both output voltages, add a resistor (R2), between $\pm V_O$ *Adj* (pin 7) and the $+V_O$ (pin 5) voltage rail; see Figure 1-1(b).

Figure 1-1b



Calculation of Resistor Adjust Values

The value of the adjust resistor is calculated using one of the following equations. Use the equation for R1 to adjust up, or (R2) to adjust down.

$$\text{R1 [Adjust Up]} = \frac{V_R\, R_O}{2\,(V_A - V_O)} - R_S \quad k\Omega$$

$$\text{(R2) [Adjust Down]} = \frac{R_o\,(2\,V_A - V_R)}{2\,(V_O - V_A)} - R_S \quad k\Omega$$

Where: V_O = Magitude of the original $\pm V_O$
V_A = Magnitude of the adjusted voltage
V_R = The reference voltage from Table 1-1
R_O = The resistance value in Table 1-1
R_S = The series resistance from Table 1-1

Table 1-1

ADJUSTMENT RANGE AND FORMULA PARAMETERS

Series Pt. No.	PTB48600A
V_O (nom)	5 V
V_A (min)	3.31 V
V_A (max)	6 V
V_R	2.495 V
R_O (kΩ)	7.5
R_S (kΩ)	9.09

Notes:

1. A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C or better. Place the resistor in either the R1 or (R2) location, as close to the converter as possible.
2. Never connect capacitors to the $\pm V_O$ *Adj* pin. Capacitance added to this pin can affect the stability of the regulated output.

Configuring the PTB48600 & PTB4850x DC/DC Converters for DSL Applications

When operated as a pair, the PTB48600 and PTB4850x converters are specifically designed to provide all the required supply voltages for powering xDSL chipsets. The PTB4850x produces two logic voltages. They include a 3.3-V source for logic and I/O, and a low-voltage for powering a digital signal processor core. The PTB48600 produces a balanced pair of complementary supply voltages that is required for the xDSL transceiver ICs. When used together in these types of applications, the PTB4850x and PTB48600 may be configured for power-up sequencing, and also synchronized to a common switch conversion frequency. Figure 2-1 shows the required cross-connects between the two converters to enable these two features.

Switching Frequency Synchronization

Unsynchronized, the difference in switch frequency introduces a beat frequency into the input and output AC ripple components from the converters. The beat frequency can vary considerably with any slight variation in either converter's switch frequency. This results in a variable and undefined frequency spectrum for the ripple waveforms, which would normally require separate filters at the input of each converter. When the switch frequency of the converters are synchronized, the ripple components are constrained to the fundamental and higher. This simplifies the design of the output filters, and allows a common filter to be specified for the treatment of input ripple.

Power-Up Sequencing

The desired power-up sequence for the AC7 supply voltages requires that the two logic-level voltages from the PTB4850x converter rise to regulation prior to the two complementary voltages that power the transceiver ICs. This sequence cannot be guaranteed if the PTB4850x and PTB48600 are allowed to power up independently, especially if the 48-V input voltage rises relatively slowly. To ensure the desired power-up sequence, the "EN Out" pin of the PTB4850x is directly connected to the active-low "Enable" input of the PTB48600 (see Figure 2-1). This allows the PTB4850x to momentarily hold off the outputs from the PTB48600 until the logic-level voltages have risen first. Figure 2-2 shows the power-up waveforms of all four supply voltages from the schematic of Figure 2-1.

Figure 2-2; Power-Up Sequencing Waveforms

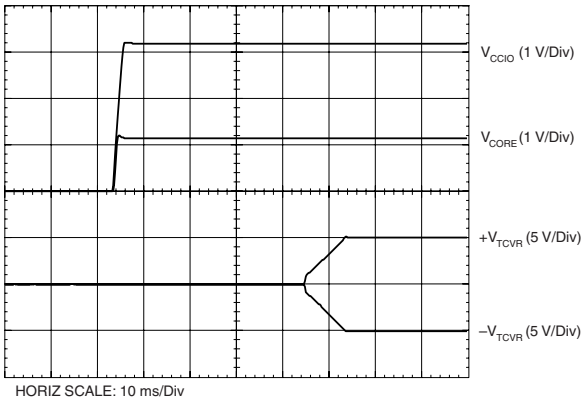
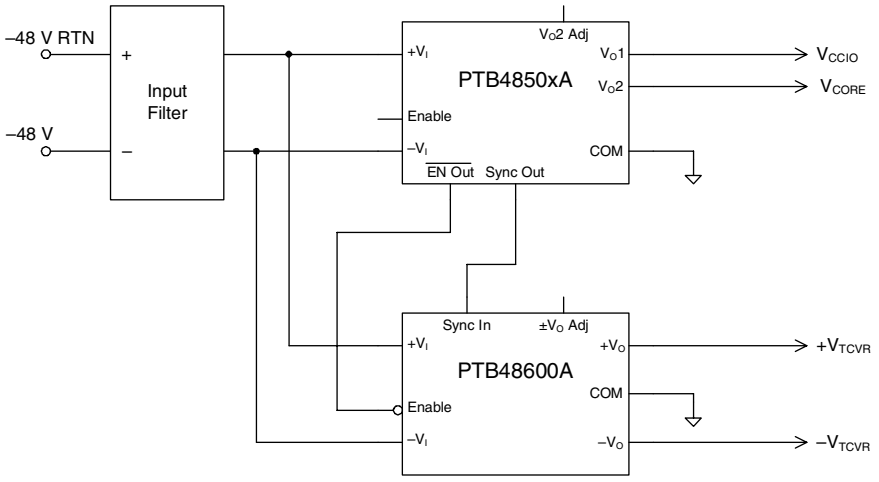


Figure 2-1; Example of PTB4850x & PTB48600 Modules Configured for DSL Applications



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTB48600AAH	NRND	Through-Hole Module	ERT	8	9	RoHS (In Work) & non-Green	SN	N / A for Pkg Type	-40 to 85		
PTB48600AAZ	NRND	Surface Mount Module	ERU	8	9	RoHS (In Work) & non-Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

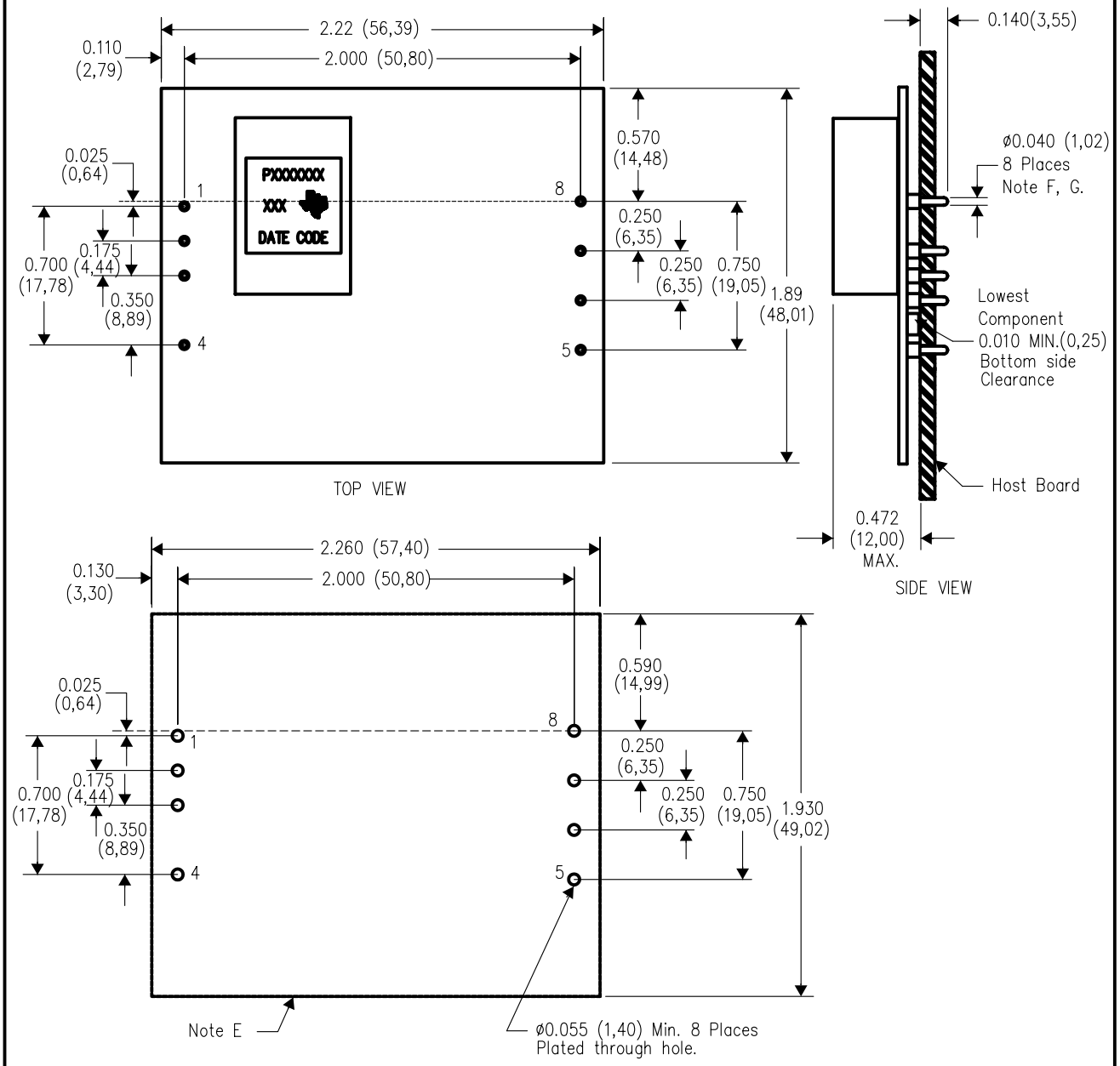
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

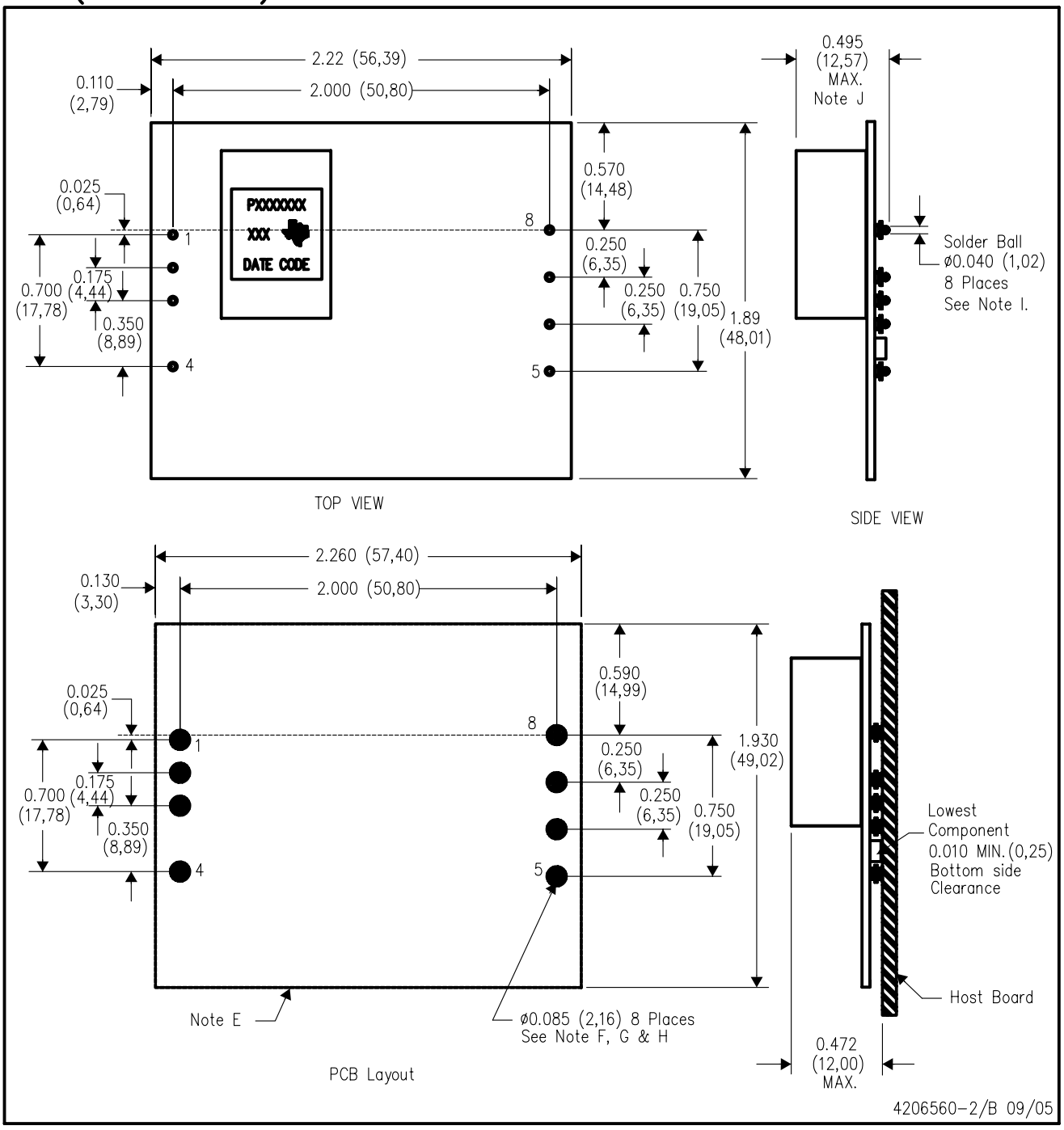
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

ERT (R–PDSS–T8) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.020 (±0,51mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

ERU (R–PDSS–T8) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.020 (±0,51mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265